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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,160	11/20/2001	Tzong-Dar Her	JCLA6875	2361

7590 05/21/2004

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EXAMINER	
LUU, CHUONG A	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/990,160	HER ET AL.	
	Examiner	Art Unit	
	Chuong A Luu	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/20/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request For Continued Examination (RCE)

The request filed on February 10, 2004 for a Request For Continued Examination (RCE) under 37 CFR 1.53(d) based on parent Application No. 09/990,160 is acceptable and a RCE has been established. An action on the RCE follows.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1, 5-6 and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Degani et al. (U.S. 5,869,894).

Degani discloses RF IC package with

(1); (12) a substrate (13);

at least a chip set of a single piece cut from a wafer, the chip set having a plurality of chips (11, 12) formed side by side with each other, wherein the chips (11, 12) are adhered on the substrate (13) and are electrically connected to the substrate (13), a plurality of circuits (14, 16) which are located on the substrate (13) not within the substrate, are located within the chip set between the chips (11, 12) and electrically connect the chips to each other (see Figures 2-3);

a molding compound, encapsulating (41) a portion of the electrical connection between the chip set (11, 12) and the substrate (13) (see column 3, lines 6-20. Figures 2-3);

(5) wherein the chip set is electrically connected to the substrate by a flip-chip technology, and the molding compound fills into a gap located between the chip set and the substrate (see Figures 2-3);

(6) wherein the chip set is electrically connected to the substrate by a plurality of conductive wires, and the molding compound encapsulates the chip set and the conductive wires (see Figures 2-3);

(13) wherein the chip set is electrically connected to the substrate by a flip-chip technology, and the molding compound fills into a gap located between the chip set and the substrate (see Figures 2-3);

(14) wherein the chip set is electrically connected to substrate by a plurality of conductive wires, and the molding compound encapsulates the chip set and the conductive wires (see Figures 2-3);

Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani et al. (U.S. 5,869,894) in view of Higgins, III (U.S. 6,064,114).

Degani teaches everything above except for wherein the substrate comprises; a plurality of patterned-trace layers; and at least an insulating layer located in between the patterned-trace layers, wherein a plurality of vias are formed in the insulating layer and electrically connect the patterned-trace layers to each other; wherein the insulating layer is made of a material selected from a group consisting of glass epoxy resin (FR-4, FR-5), bismaleimide-triazine (BT), epoxy resin or polyimide; wherein the line-patterned layers are formed by defining copper foil using photolithography. However, Higgins, III discloses a semiconductor device with **(2)** wherein the substrate comprises; a plurality of patterned-trace layers; and at least an insulating layer located in between the patterned-trace layers, wherein a plurality of vias are formed in the insulating layer and electrically connect the patterned-trace layers to each other (see Figures 1-2); **(3)** wherein the insulating layer is made of a material selected from a group consisting of polyimide (see column 3, lines 16-27); **(4)** wherein the line-

patterned layers are formed by defining copper foil using photolithography. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the flip chip device of Degani (accordance with the teaching of Higgins, III). Doing so would facilitate the manufacture of the semiconductor structure and increase its performance.

Claims 7-11 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani et al. (U.S. 5,869,894).

Degani discloses the claimed invention except for wherein the chip set comprises a total number of chips in the DCA memory module. It would have been an obvious matter of design choice to select the total number of chips in a set during fabrication a semiconductor structure to exceed its performance criteria, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955) and Nerwzn v. Erlichman, 168 USPQ 177, 179.

Claims 1, 5-6 and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Palmer et al. (U.S. 6,052,287).

Palmer discloses silicon ball grid array chip carrier with

(1); (12) a substrate (100);

at least a chip set of a single piece cut from a wafer, the chip set having a plurality of chips (10) formed side by side with each other, wherein the chips are

adhered on the substrate (100) and are electrically connected to the substrate (100), a plurality of circuits (102) which are located on the substrate not within the substrate (100), are located within the chip set between the chips (10) and electrically connect (18, 22) the chips to each other (see Figure 1);

a molding compound, encapsulating a portion of the electrical connection between the chip set (10) and the substrate (100) (see column 7, lines 1-9. Figure 1);

(5) wherein the chip set is electrically connected to the substrate by a flip-chip technology, and the molding compound fills into a gap located between the chip set and the substrate (see Figure 1);

(6) wherein the chip set is electrically connected to the substrate by a plurality of conductive wires, and the molding compound encapsulates the chip set and the conductive wires (see Figure 1);

(13) wherein the chip set is electrically connected to the substrate by a flip-chip technology, and the molding compound fills into a gap located between the chip set and the substrate (see Figure 1);

(14) wherein the chip set is electrically connected to substrate by a plurality of conductive wires, and the molding compound encapsulates the chip set and the conductive wires (see Figure 1);

Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palmer et al. (U.S. 6,052,287). in view of Higgins, III (U.S. 6,064,114).

Palmer teaches everything above except for wherein the substrate comprises; a plurality of patterned-trace layers; and at least an insulating layer located in between the patterned-trace layers, wherein a plurality of vias are formed in the insulating layer and electrically connect the patterned-trace layers to each other; wherein the insulating layer is made of a material selected from a group consisting of glass epoxy resin (FR-4, FR-5), bismaleimide-triazine (BT), epoxy resin or polyimide; wherein the line-patterned layers are formed by defining copper foil using photolithography. However, Higgins, III discloses a semiconductor device with **(2)** wherein the substrate comprises; a plurality of patterned-trace layers; and at least an insulating layer located in between the patterned-trace layers, wherein a plurality of vias are formed in the insulating layer and electrically connect the patterned-trace layers to each other (see Figures 1-2); **(3)** wherein the insulating layer is made of a material selected from a group consisting of polyimide (see column 3, lines 16-27); **(4)** wherein the line-patterned layers are formed by defining copper foil using photolithography. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the semiconductor device of Palmer (accordance with the teaching of Higgins, III). Doing so would facilitate the manufacture of the semiconductor structure and increase its performance.

Claims 7-11 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palmer et al. (U.S. 6,052,287).

Palmer discloses the claimed invention except for wherein the chip set comprises a total number of chips in the DCA memory module. It would have been an obvious matter of design choice to select the total number of chips in a set during fabrication a semiconductor structure to exceed its performance criteria, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955) and Nerwzn v. Erlichman, 168 USPQ 177, 179.

Claims 1, 5-6 and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Akram et al. (U.S. 5,994,166).

Akram discloses a method of constructing stacked packages with

(1); (12) a substrate (116);

at least a chip set of a single piece cut from a wafer, the chip set having a plurality of chips (128) formed side by side with each other, wherein the chips are adhered on the substrate (116) and are electrically connected to the substrate (116), a plurality of circuits (160, 158 and 154) which are located on the substrate not within the substrate, are located within the chip set between the chips (128) and electrically connect (138) the chips to each other (see column 6, lines 37-54. Figure 1);

a molding compound, encapsulating (170) a portion of the electrical connection between the chip set (128) and the substrate (116) (see Figure 1);

(5) wherein the chip set is electrically connected to the substrate by a flip-chip technology, and the molding compound fills into a gap located between the chip set and the substrate (see Figure 1);

(6) wherein the chip set is electrically connected to the substrate by a plurality of conductive wires, and the molding compound encapsulates the chip set and the conductive wires (see Figure 1);

(13) wherein the chip set is electrically connected to the substrate by a flip-chip technology, and the molding compound fills into a gap located between the chip set and the substrate (see Figure 1);

(14) wherein the chip set is electrically connected to substrate by a plurality of conductive wires, and the molding compound encapsulates the chip set and the conductive wires (see Figure 1);

Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al. (U.S. 5,994,166) in view of Higgins, III (U.S. 6,064,114).

Akram teaches everything above except for wherein the substrate comprises; a plurality of patterned-trace layers; and at least an insulating layer located in between the patterned-trace layers, wherein a plurality of vias are formed in the insulating layer and electrically connect the patterned-trace layers to each other; wherein the insulating layer is made of a material selected from a group consisting of glass epoxy resin (FR-4, FR-5), bismaleimide-triazine (BT), epoxy resin or polyimide; wherein the line-patterned layers are formed by defining copper foil using photolithography.

However, Higgins, III discloses a semiconductor device with **(2)** wherein the substrate comprises; a plurality of patterned-trace layers; and at least an insulating layer located in between the patterned-trace layers, wherein a plurality of vias are formed in the insulating layer and electrically connect the patterned-trace layers to each other (see Figures 1-2); **(3)** wherein the insulating layer is made of a material selected from a group consisting of polyimide (see column 3, lines 16-27); **(4)** wherein the line-patterned layers are formed by defining copper foil using photolithography. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to combine the above teachings to fabricate a semiconductor device to exceed its performance criteria.

Claims 7-11 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al. (U.S. 5,994,166).

Akram discloses the claimed invention except for wherein the chip set comprises a total number of chips in the DCA memory module. It would have been an obvious matter of design choice to select the total number of chips in a set during fabrication a semiconductor structure to exceed its performance criteria, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955) and Nerwzn v. Erlichman, 168 USPQ 177, 179.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1975.

CARIDAD EVERHART
PRIMARY EXAMINER

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May 17, 2004